

# DF1-xxSxxLT Series

DC-DC Converter | 1W | SMD12 | Fixed voltage input, unregulated output | 3000VDC



## Features

- Compact SMD12 Package
- Operating Temperature Range: -40°C ~ +105°C
- Isolation Voltage: 3000VDC
- Full Load Efficiency: up to 89% (typ.)
- Continuous Short Circuit Protection
- Designed to meet IEC/EN/BS EN/UL 62368

## Product Description



The DF1-xxSxxLT series is 1W unregulated DC/DC converters that are an ideal and economical solutions for on-board power applications where an isolated voltage is required. Typical applications are digital interfaces, voltage conversion in distributed power systems, general low-frequency analog circuits, relay drive circuits, data exchange circuits, etc. For automated SMD production lines, this series can be supplied in standard tape and reel package.

## Selection Guide

Certification	Part No.	Input Voltage	Output			Full Load Efficiency (%) Typ.	Capacitive Load(μF) Max.
		Nominal (Range) (VDC)	Voltage (VDC)	Current (mA) Min.	Current (mA) Max.		
EN/UL Pending	DF1-03S03LT	3.3 (2.97~3.63)	3.3	30	303	82	2400
	DF1-03S05LT	3.3 (2.97~3.63)	5	20	200	83	2400
	DF1-03S09LT	3.3 (2.97~3.63)	9	11	111	84	1000
	DF1-03S12LT	3.3 (2.97~3.63)	12	8	84	85	560
	DF1-03S15LT	3.3 (2.97~3.63)	15	7	67	85	560
	DF1-03S24LT	3.3 (2.97~3.63)	24	4	42	85	220
	DF1-05S03LT	5 (4.5~5.5)	3.3	30	303	80	2400
	DF1-05S05LT	5 (4.5~5.5)	5	20	200	84	2400
	DF1-05S09LT	5 (4.5~5.5)	9	11	111	86	1000
	DF1-05S12LT	5 (4.5~5.5)	12	8	84	89	560
	DF1-05S15LT	5 (4.5~5.5)	15	7	67	88	560
	DF1-05S24LT	5 (4.5~5.5)	24	4	42	88	220
	DF1-12S03LT	12 (10.8~13.2)	3.3	30	303	83	2400

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Certification	Part No.	Input Voltage	Output			Full Load Efficiency (%) Typ.	Capacitive Load(μF) Max.
		Nominal (Range) (VDC)	Voltage (VDC)	Current (mA) Min.	Current (mA) Max.		
EN/UL Pending	DF1-12S05LT	12 (10.8~13.2)	5	20	200	86	2400
	DF1-12S09LT	12 (10.8~13.2)	9	11	111	89	1000
	DF1-12S12LT	12 (10.8~13.2)	12	8	84	89	560
	DF1-12S15LT	12 (10.8~13.2)	15	7	67	89	560
	DF1-12S24LT	12 (10.8~13.2)	24	4	42	89	220
	DF1-15S03LT	15 (13.5~16.5)	3.3	30	303	82	2400
	DF1-15S05LT	15 (13.5~16.5)	5	20	200	85	2400
	DF1-15S09LT	15 (13.5~16.5)	9	11	111	88	1000
	DF1-15S12LT	15 (13.5~16.5)	12	8	84	89	560
	DF1-15S15LT	15 (13.5~16.5)	15	7	67	89	560
	DF1-15S24LT	15 (13.5~16.5)	24	4	42	89	220
	DF1-24S03LT	24 (21.6~26.4)	3.3	30	303	84	2400
	DF1-24S05LT	24 (21.6~26.4)	5	20	200	87	2400
	DF1-24S09LT	24 (21.6~26.4)	9	11	111	89	1000
	DF1-24S12LT	24 (21.6~26.4)	12	8	84	88	560
	DF1-24S15LT	24 (21.6~26.4)	15	7	67	89	560
	DF1-24S24LT	24 (21.6~26.4)	24	4	42	89	220

Note: The above efficiency is measured at nominal input voltage and rated output load.

## Input Specifications

Item	Operating Conditions		Min.	Typ.	Max.	Unit	
Input Current (Full Load/No-load)	3.3VDC Input	3.3VDC Output	--	370/10	389/15	mA	
		Others	--	365/12	384/18	mA	
	5VDC Input	3.3VDC Output	--	250/8	264/15	mA	
		5VDC Output	--	238/10	250/15	mA	
		9VDC Output	--	233/10	244/15	mA	
		12/15/24VDC Output	--	227/18	239/25	mA	
	12VDC Input	3.3VDC Output	--	100/7	106/15	mA	
		5VDC Output	--	97/7	102/15	mA	
		Others	--	94/8	99/15	mA	
	15VDC Input	3.3VDC Output	--	82/6	86/15	mA	
		5VDC Output	--	78/6	83/15	mA	
		Others	--	76/6	80/15	mA	
	24VDC Input	3.3VDC Output	--	50/3	53/15	mA	
		Others	--	48/4	51/15	mA	
	Reflected Ripple Current			--	15	--	mA
	Surge Voltage	3.3VDC Input		-0.7	--	5	VDC
5VDC Input		-0.7	--	9	VDC		
12VDC Input		-0.7	--	18	VDC		
15VDC Input		-0.7	--	21	VDC		
24VDC Input		-0.7	--	30	VDC		
Input Filter Type			Capacitance Filter				
Hot Plug			Unavailable				

## Output Specifications

Item	Operating Conditions		Min.	Typ.	Max.	Unit
Output Voltage Accuracy			See Output Regulation Curve			
Line Regulation	Rated Load	3.3V	--	±1.5	--	%
		Others	--	±1.2	--	%
Load Regulation	10%~100% Load	3.3VDC Output	--	10	--	%
		5VDC Output	--	10	--	%
		9VDC Output	--	8	--	%
		12VDC Output	--	8	--	%
		15VDC Output	--	8	--	%
		24VDC Output	--	6	--	%
Ripple & Noise	20MHz Bandwidth (Peak-to-Peak)		--	45	120	mVp-p
Temperature Coefficient	Full Load		--	±0.02	--	%/°C
Short Circuit Protection			Continuous, Self-Recovery			

Note: Ripple & noise are measured at 20MHz of bandwidth with a 10uF electrolytic capacitor and a 1uF ceramic capacitor connected in parallel at the output.

## General Specifications

Item	Operating Conditions	Min.	Typ.	Max.	Unit
Isolation Voltage	Input-output, test time 1 minute, leakage current less than 1mA	3000	--	--	VDC
Insulation Resistance	Input-output, insulated voltage 500VDC	1000	--	--	MΩ
Isolation Capacitance	Input-Output, 100KHz/0.1V	--	20	--	pF
Operating Temperature	Derating when operating temperature $\geq 85^{\circ}\text{C}$ (See Temperature derating curve chart)	-40	--	105	$^{\circ}\text{C}$
Storage Temperature		-55	--	125	$^{\circ}\text{C}$
Case Temperature Rise	$T_a=25^{\circ}\text{C}$ , Nominal Input, Full Load	--	25	--	$^{\circ}\text{C}$
Storage Humidity	Non-condensing	5	--	95	%RH
Reflow Soldering Temperature	Peak temperature $T_c \leq 245^{\circ}\text{C}$ , maximum time above $217^{\circ}\text{C}$ is 60 seconds				
Switching Frequency	Full Load, Nominal Input Voltage	--	220	--	kHz
MTBF	MIL-HDBK-217F@ $25^{\circ}\text{C}$	>3500Kh			

## Mechanical Specifications

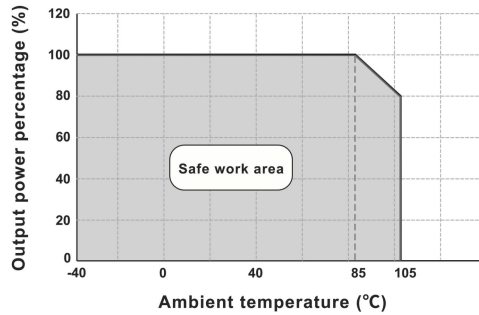
Case Material	Black flame-retardant heat-resistant plastic (UL94V-0)
Mechanical Dimensions	15.24 * 11.40 * 7.25 mm
Weight	1.7g(typ.)
Cooling Method	Free air convection

## Electromagnetic Compatibility (EMC)

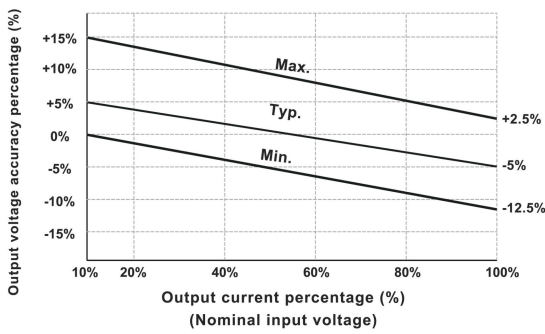
EMI	CE	CISPR32/EN55032 CLASS B (EMC recommended circuit see Fig. 2)
	RE	CISPR32/EN55032 CLASS B (EMC recommended circuit see Fig. 2)
EMS	ESD	IEC/EN61000-4-2 Contact $\pm 6\text{KV}$ , Air $\pm 8\text{KV}$ perf. Criteria B

Product Characteristic Curve

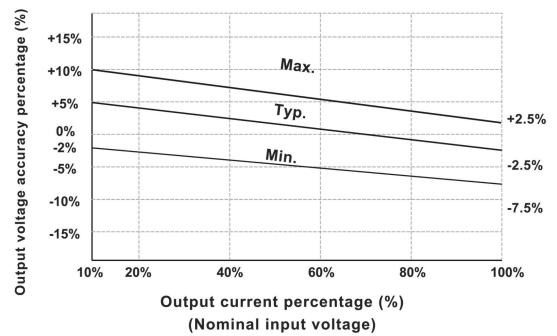
Temperature Derating Curve



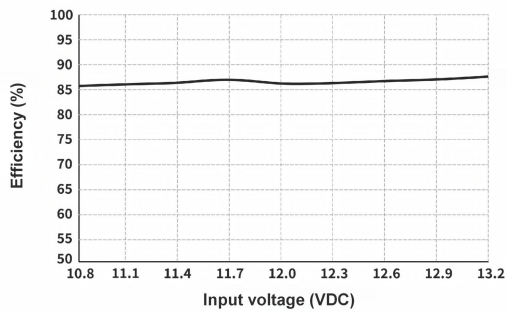
Error Envelope Curve (3.3V Output)



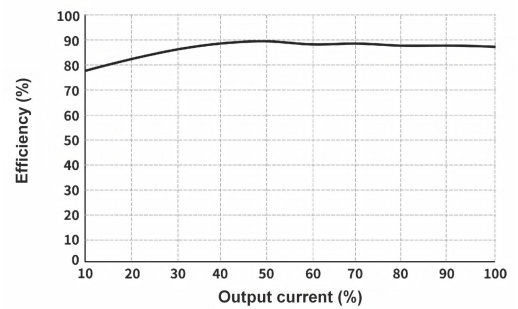
Output Regulation Curve (Others)



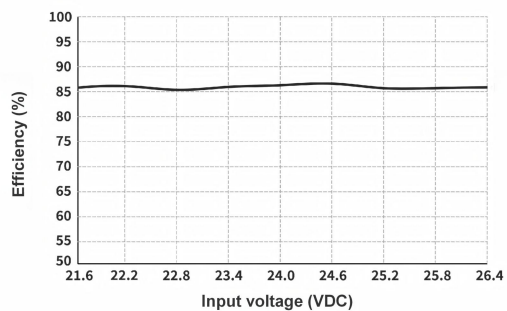
Efficiency vs Input Voltage (Full Load, DF1-12S12LT)



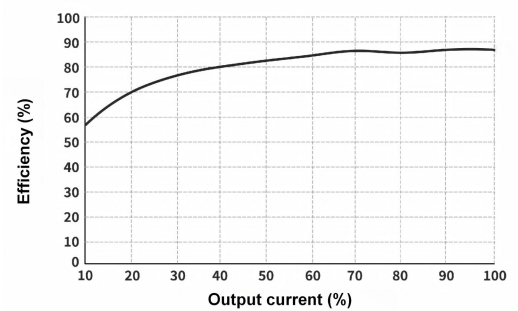
Efficiency vs Output Load (Vin=12V, DF1-12S12LT)



Efficiency vs Input Voltage (Full Load, DF1-24S12LT)

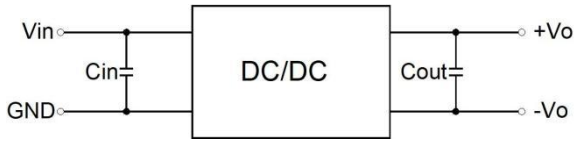


Efficiency vs Output Load (Vin=24V, DF1-24S12LT)



## Design Reference - Application Circuit

Application circuit



(Figure 1)

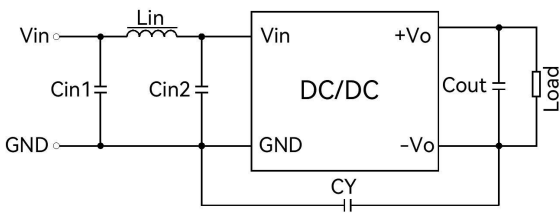
Recommended Capacitive Load Value Table

Vin	Cin	Vo	Cout
3.3/5VDC	4.7uF/16V	3.3/5VDC	10uF/16V
12VDC	2.2uF/25V	9/12VDC	4.7uF/25V
15VDC	1.0uF/25V	15VDC	1.0uF/25V
24VDC	1.0uF/50V	24VDC	0.47uF/50V

All DC/DC converters in this series are tested according to the recommended test circuit (Figure 1) before leaving the factory. If further reduction of input and output ripple is required, the external capacitors Cin and Cout can be increased or capacitors with lower series equivalent impedance can be selected. For each output, under safe and reliable operating conditions, the maximum capacitance of the filter capacitor must not exceed the maximum capacitive load of the product.

## Design Reference - EMC Solutions - Recommended Circuits

EMC Recommended Circuit Design and Application



(Figure 2)

Recommended Parameter Table

Cin1	4.7μF /50V
Cin2	4.7μF /50V
Cout	Refer to the Cout parameter in Figure 1
CY	1000pF/2kVDC
Lin	6.8μH

Note:

### 1. Typical Application

To further reduce input and output ripple, a Capacitance Filter network can be connected at the input and output terminals. The application circuit is shown in Figure 1. However, care should be taken to select an appropriate filter capacitor. If the capacitor is too large, it may cause startup issues. For each output, under conditions ensuring safe and reliable operation, the recommended capacitive load values are detailed in the table.

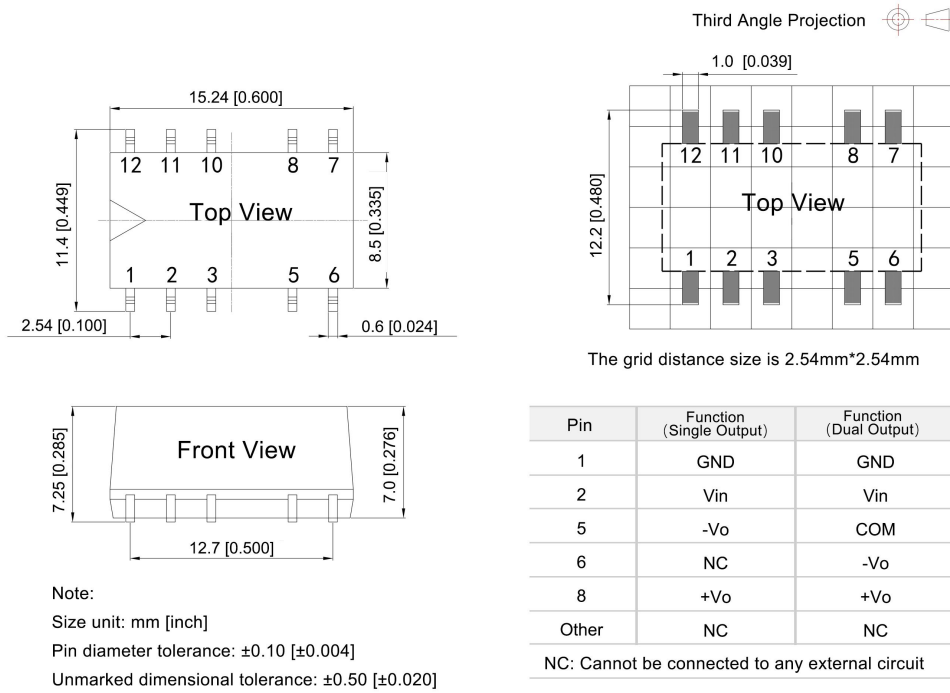
### 2. EMC Recommended Circuit: See Figure 2

### 3. Output Load Requirements

To ensure the module operates efficiently and reliably, the minimum output load during use must not be less than 10% of the rated load. If the required power is indeed very small, please connect a resistor in parallel at the output (the sum of the resistor's power dissipation and the actual usage power must be greater than or equal to 10% of the rated power).

## Dimensions and Recommended Layout

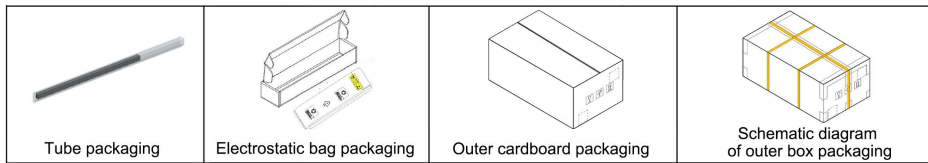
DF1-xxSxxLT Dimensions and Recommended Layout



## Packaging Information

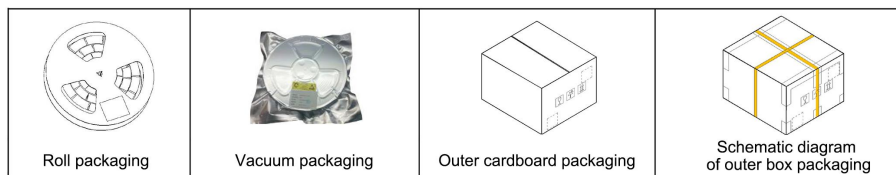
Model series (Tube packaging)	Quantity per tube (pcs/ tube)	Quantity of electrostatic bag (pcs/ bag)	Quantity of inner box (pcs/ box)	Full box Quantity (pcs)
DF1-xxSxxLT	38	760	3040	12160

The schematic diagram of tube packaging is shown below:

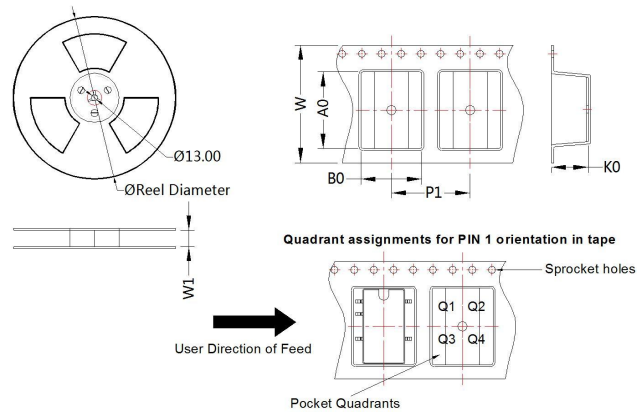


Model series (Reel packaging)	Quantity of products carried (pcs/ROLL)	Quantity of electrostatic bag (pcs/ bag)	Quantity of inner box (pcs/ box)	Full box Quantity (pcs)
DF1-xxSxxLT	500	500	1500	3000

The schematic diagram of Reel packaging is shown below:



Package type	Pin	MPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Pin1 Quadrant
SMD	10	500	330	24.5	15.6	12.4	7.45	16	24	Q1



## Product precautions

1. The input voltage should not exceed the specified range value, otherwise it may cause permanent and irreparable damage;
2. It is recommended to use at a load of over 5%. If the load is below 5%, the ripple index of the product may exceed the specifications, but it does not affect the reliability of the product;
3. The maximum capacitive load is tested within the input voltage range and under full load conditions;
4. Unless otherwise specified, all indicators in this manual are measured at  $T_a=25\text{ }^\circ\text{C}$ , humidity<75% RH, nominal input voltage, and output rated load;
5. All indicator testing methods in this manual are based on our company's corporate standards;
6. Our company can provide product customization, and specific requirements can be directly contacted by our technical personnel;
7. Product specifications are subject to change without prior notice.

## Manufacturer contact information

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